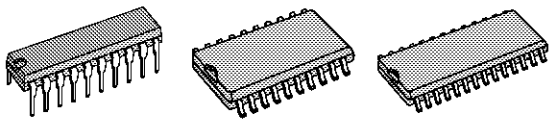
SGS-THOMSON MICROELECTRONICS

TDA7327

AM-FM RADIO FREQUENCY SYNTHESIZER AND IF COUNTER

ADVANCE DATA

- FM INPUT AND PRECOUNTER FOR UP TO 160MHz
- AM INPUT FOR UP TO 64MHz
- ON CHIP LOOP FILTER
- TWO SEPARATE FREE PROGRAMMABLE FILTERS APPLICATIONS AVAILABLE
- TUNING VOLTAGE OUTPUT 0.5 TO 9V
- PROGRAMMABLE CURRENT SOURCES TO SET THE LOOP GAIN
- IF COUNTER FOR FM, AM UP-CONVERSION AND NORMAL MODE
- VARIABLE SAMPLING TIME VALUES
- ADJUSTABLE CENTER FREQUENCY VALUES
- I^2C BUS INTEFACE
- ON-CHIP REFERENCE OSCILLATOR AND COUNTER
- TWO OR NINE DIGITAL OUTPUTS (NINE DIGITAL OUTPUTS AT THE 28 PIN VERSION)



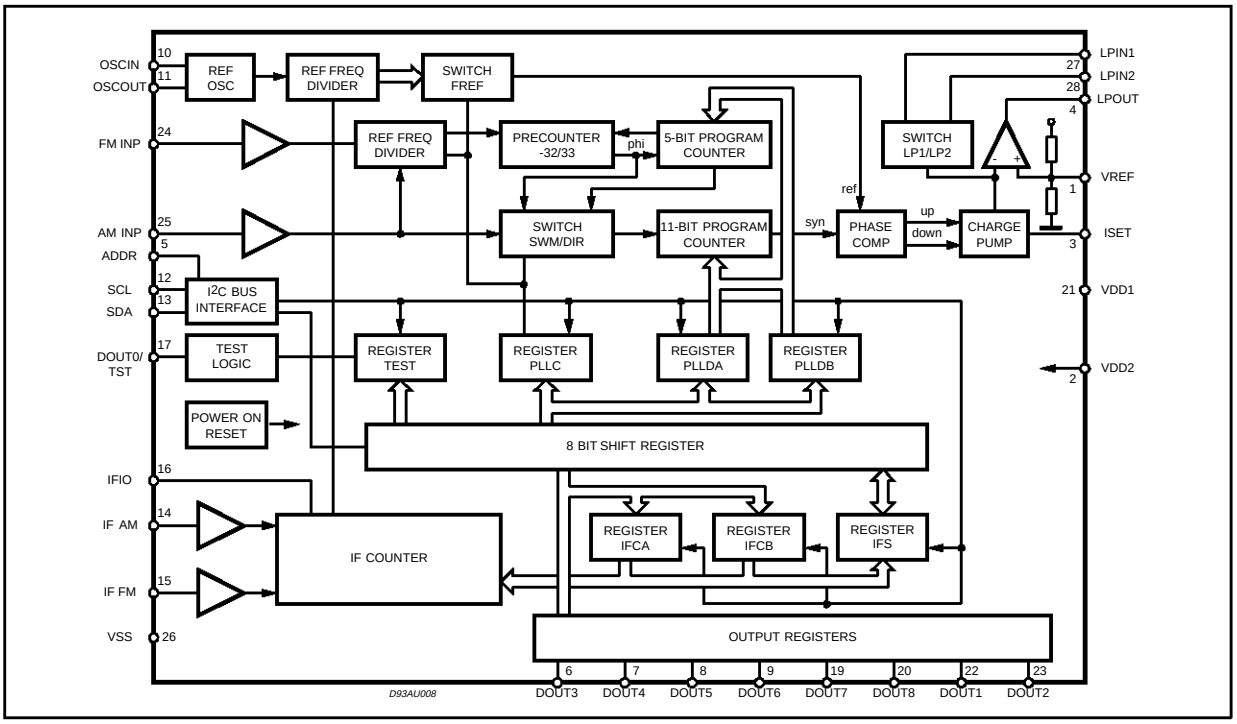
DIP20 **SO20** **SO28**

ORDERING NUMBER: TDA7327 (DIP20)
TDA7327D (SO20)
TDA7327D1 (SO28)

DESCRIPTION

The TDA7327 is a PLL frequency synthesizer with an additional IF-counting system that performs all the function of a PLL radio tuning system for FM and AM (LW, MW, SW) including the IF-counter for the search stop function.

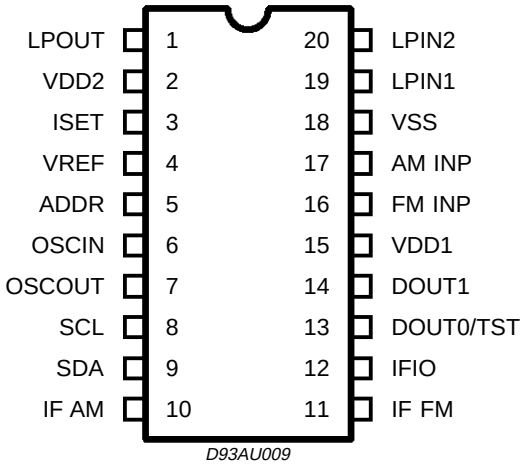
BLOCK DIAGRAM



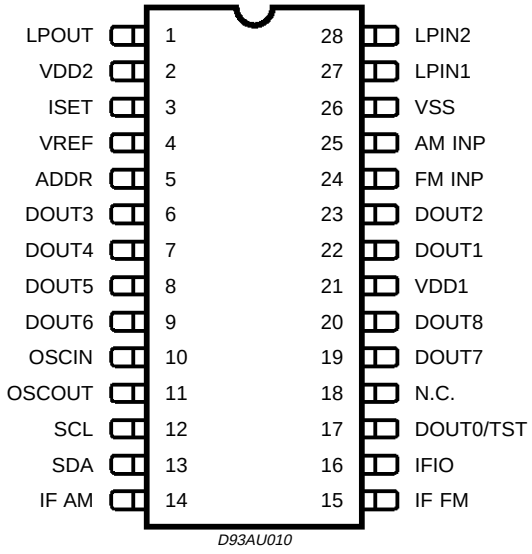
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD1} - V_{SS}	Supply Voltage	- 0.3 to + 7	V
V_{DD2} - V_{SS}	Supply Voltage	- 0.3 to + 12	V
V_{IN}	Input Voltage	VSS - 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	VSS - 0.3 to V_{DD} + 0.3	V
I_{IN}	Input Current	- 10 to + 10	mA
I_{OUT}	Output Current	- 10 to + 10	mA
P_{tot}	Total Power Dissipation	300	mW
T_{stg}	Storage Temperature	- 55 to + 125	^{o}C
T_{amb}	Ambient Temperature	-40 to + 85	^{o}C

PIN CONNECTIONS



DIP20/SO20L



SO28

THERMAL DATA

Symbol	Parameter	DIP 20	SO 20L	SO 28	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	100	150	200	^{o}C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C ; V_{DD1} - V_{SS} = 5V; V_{DD2} - V_{SS} = 9V; f_{OSC} = 4MHz; R_{ISET} = 22KΩ; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage		4.5	5.0	5.5	V
V_{DD2}	Supply Voltage			9.0	10.0	V
$I_{DD1\ FM}$	Supply Current	no output load, FM mode,		20		mA
$I_{DD1\ AM}$	Supply Current	no output load, AM mode,		6		mA
$I_{DD1\ STB}$	Supply Current	Standby mode			30	µA
V_{REF}	Voltage at VREF pin			3.5		V
V_{ISET}	Voltage at ISET pin			8.0		V
RF INPUT (AMIN, FMIN)						
f_{iMIN}	Min Input Frequency AM	Direct Mode			0.5	MHz
		Swallow Mode			16	MHz
f_{iMAX}	Max Input Frequency AM	Direct Mode	20			MHz
		Swallow Mode	64			MHz
f_{iMIN}	Min Input Frequency FM	Sinus			30	MHz
f_{iMAX}	Max Input Frequency FM	Sinus	160			MHz
V_{iMIN}	Min Input Voltage AM	Direct Mode 0.6 to 16MHz (Sinus)			40	mV/rms
		Swallow Mode 16 to 40MHz (Sinus)			40	mV/rms
V_{iMAX}	Max Input Voltage AM	0.6 to 64MHz (Sinus)	600			mV/rms
V_{iMIN}	Min Input Voltage FM	70 to 120MHz (Sinus)			30	mV/rms
V_{iMAX}	Max Input Voltage FM	70 to 120MHz (Sinus)	600			mV/rms
Z_{in}	Input Impedance FM	fin = 120MHz		200		Ω
Z_{in}	Input Impedance AM	f_{in} = 12MHz		1400		Ω
IF COUNTER						
f_{iMAX}	Max Input Frequency AMIF	Sinus	500			KHz
f_{iMAX}	Max Input Frequency FMIF	Sinus	11			MHz
f_{iMIN}	Min Input Frequency AMIF	Sinus			400	KHz
f_{iMIN}	Min Input Frequency FMIF	Sinus			10	MHz
V_{iMIN}	Min Input Voltage AMIF	Sinus			100	mV/rms
V_{iMIN}	Min Input Voltage FMIF	Sinus			100	mV/rms
V_{iMAX}	Max Input Voltage AMIF	Sinus	600			mV/rms
V_{iMAX}	Max Input Voltage FMIF	Sinus	600			mV/rms
V_{iMAX}	Input Inpedance FMIF	fin =10.7MHz		2000		Ω
Z_{in}	Input Inpedance AMIF	f_{in} =455KHz		4000		Ω
		f_{in} =10.7MHz		2000		Ω
IFIO I/O						
$-I_{IL}$	Input Leakage Current	$V_{in} = V_{SS}$	-10		10	µA
I_{IH}	Input Leakage Current	Vin = V_{DD}	-10		10	µA
V_{IH}	Input Voltage High	Leading Edge	3.4			V
V_{IL}	Input Voltage Low	Trailing Edge			1.6	V
DOUT OUTPUT (D_{OUT0}.....$D_{OUT\ 8}$)						
V_{OL}	Output Voltage Low	I = 2mA			0.5	V
V_{OH}	Output Voltage High	I = 2mA; VDD1 = 5V	9.5			V

ELECTRICAL CHARACTERISTICS (continued)

BUS INTERFACE

T_j	Noise Suppression Time Constant on SCL, SDA Input				100	ns
f_{SCL}	SCL Clock Frequency		0		100	kHz
t_{AA}	SCL Low to SDA Data Valid		300			ns
t_{buf}	Time the Bus Must Be Free for the New Transmission		4.7			µs
t_{HD-STA}	START Condition hold Time		4.0			µs
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{SU-SDA}	Start Condition Setup Time		4.7			µs
t_{HD-DAT}	Data Input Hold Time		0		1	µs
t_{SU-DAT}	Date Input Setup Time		250		300	ns
t_R	SDA & SCL Rise Time			TBD		µs
t_F	SDA & SCL Full Time			TBD		µs
t_{SU-STO}	Stop Condition Setup Time		4.7			µs
t_{DH}	DATA OUT Time		300			ns

OSCILLATOR

f_{OSC}	Oscillator Frequency	Euro-Quartz ITT		4		MHz
t_{bu}	Build Up Time				100	ms
C_{in}	Internal Capacitance			9		pF
C_{OUT}	Internal Capacitance			9		pF
Z_{in}	Input Impedance	f_{osc} = 4MHz			100	KΩ
V_{in}	Min Input Voltage (for Slave Mode)	f_{IN} = 4MHz			10	mV
V_{in}	Max Input Voltage (for Slave Mode)	f_{IN} = 4MHz	300			mV

LOOP FILTER INPUT OUTPUT (LPIN1, LPIN2, LPOUT)

$-I_{IN}$	Input Leakage Current	$V_{IN} = V_{SS}$; PD_{out} = Tristate		-0.1		µA
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$; PD_{out} = Tristate		0.1		µA
V_{OL}	Output Voltage Low	I_{IN} = -0.2mA			0.5	V
V_{OH}	Output Voltage High	I_{OUT} = 0.2mA; V_{DD2} = 10V	9			V
I_{OUT}	Output Current	V_{DD} = 10V; V_{out} = 0.5 to 8.5V		±10		mA

2.1 GENERAL DESCRIPTION

This circuit contains a frequency synthesizer and a loop filter for an FM and AM radio tuning system. Only a V_{CO} is required to build a complete PLL system. For auto search stop operation an IF counter system is available.
A small signal of the AM and FM V_{CO} can be accepted by the circuit.
For FM and SW application, the counter works in a two stages configuration.
The first stage is a swallow counter with a two modulus (:32/33) precounter.
The second stage is an 11-bit programmable counter.
For LW and MW application, a 16-bit programmable counter is available.
The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via a I^2C bus interface.
The reference frequency is generated by a 4MHz XTAL oscillator followed by the reference divider.
An external oscillator (f = 4MHz) can be used instead of the internal one; it must be connected to OSCIN.
The reference- and step-frequency is 1, 2, 2.5, 5kHz for AM.
For FM mode a step frequency of 6.25, 12.5, 25 or 50kHz can be selected.
The circuit checks the format of the received data words.
Valid data in the interface shift register are stored automatically in buffer registers at the end of transmission.
The output signals of the phase detector are switching the programmable current sources.
Their currents are integrated in the loop filter to a DC voltage.The values of the current sources are programmable by two bits also received via the serial bus.
The loop gain can be set for different conditions.
In standby mode, oscillator, reference counter, AM input and FM input are stopped. The power consumption is reduced to a minimum.

2.2 DESCRIPTION OF THE IF-COUNTER SYSTEM

Two separate inputs are available for AM and FM IF signals. The grade of integration is adjustable by six different measuring cycle times.
The tolerance of the accepted count value is adjustable in four steps, to reach an optimum compromise for search speed and precision of the evaluation.
For the FM range the center frequency of the measured count value is adjustable in 64 steps, to get the possibility of fitting the IF-filter tolerance. In the AM range an IF frequency of 450 to 466KHz with 1KHz steps is available. For up-conversion application, an IF center frequency of 10.7MHz plus/minus eight 1KHz steps is available.

3.0 DETAILED DESCRIPTION OF THE DEVICE

3.1 THE PLL FREQUENCY SYNTHESIZER

3.1.1 Input Amplifiers

The signals applied on AM and FM input are amplified to get a logic level in order to drive the frequency dividers.

3.1.1.1 Input Impedance

The typical input impedance: for the FM input is 200Ω and for AM input is 1.4kΩ.

3.1.2.1 REGISTER LOCATION

		MSB							LSB
SYSTEM	**SUBAD**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
General	00h	/DOUT8	/DOUT7	/DOUT6	/DOUT5	/DOUT4	/DOUT3	/DOUT2	/DOUT1
PLL	07h	PC2	PC1	PC0	SC4	SC3	SC2	SC1	SC0
	06h	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3
	05h	UPC	REF2	REF1	LPF1/2	CURR2	CURR1	SWM/DIR	AM/FM
IF-COUNTER	03h	IFCA0	IFCA1	IFCA2	IFCA3	IFCA4	IFCA5		
	02h	IFCB0	IFCB1	IFCB2	IFCB3	IFCB4			
	01h	IFS0	IFS1	IFS2	IFS3	IFS4	IFS5	IFS6	IFS7
TEST	04h					DOUT0	TEST2	TEST1	TEST0

3.1.2.2 CONTROL AND STATUS REGISTERS

REGISTER NAME	FUNCTION
SWM/DIR	Swallow direct-mode switch 1 = SWM, 0 = DIR
AM/FM	AM - FM band switch 1=AM, 0 = FM
f_{REF1}, f_{REF2}	Selection of reference frequency (see table 3.4)
CURR1	Current select of change pump
CURR2	Current select of change pump
LPF1/LPF2	Loop filter input select 1= I_{PF1}, 0 = I_{PF2}
DOUT 0...8	Digital Switch output 0.....8

Figure 2: FM and AM (SW) operation (swallow mode)

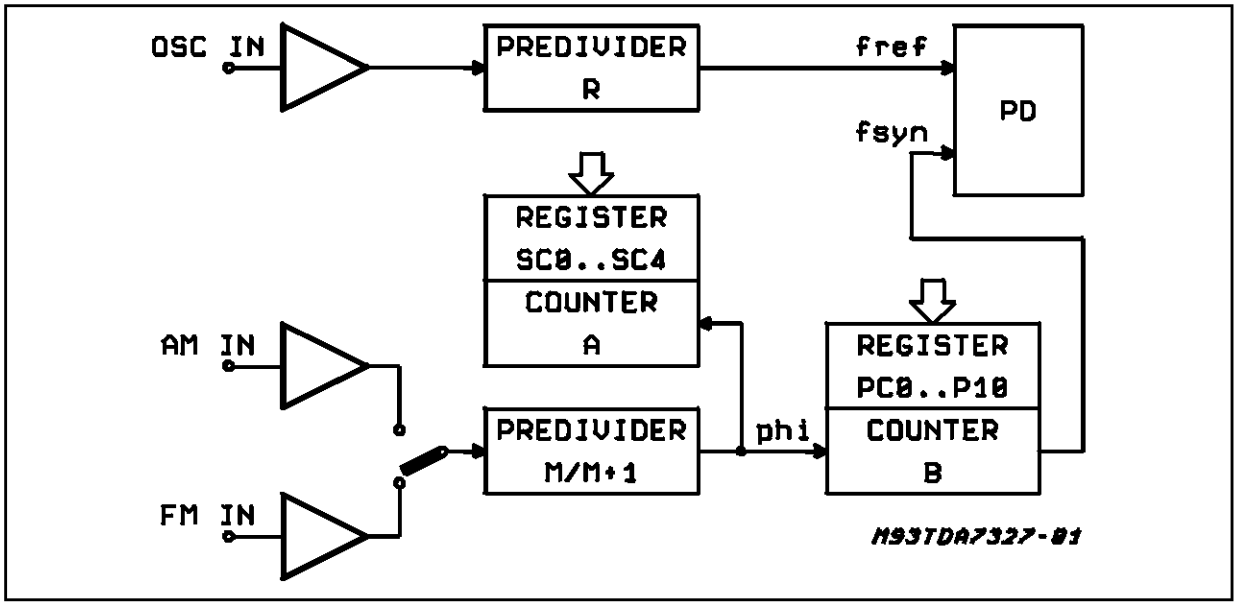
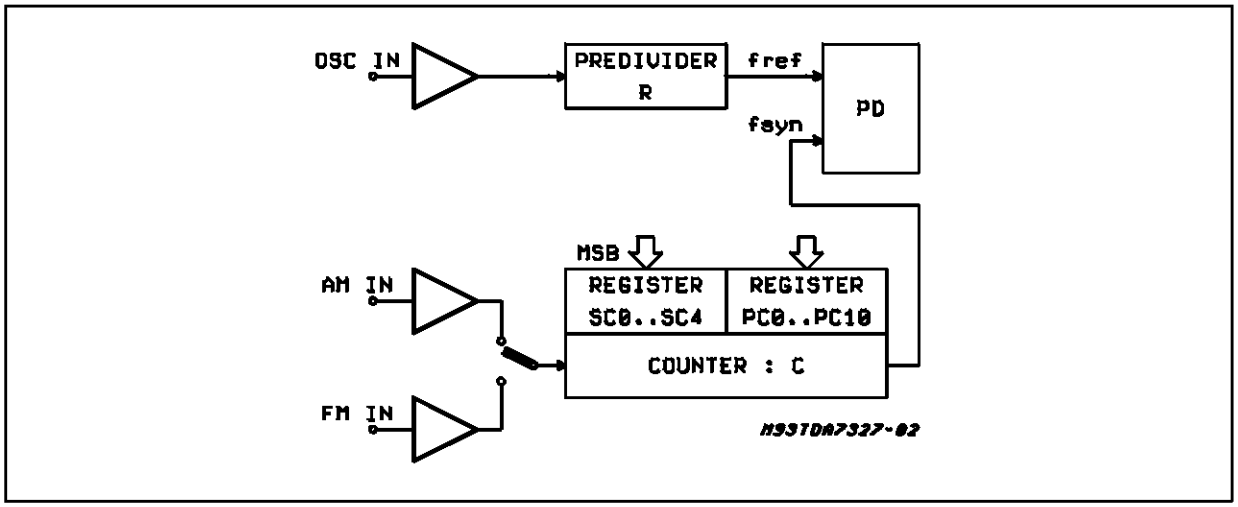


Figure 3: AM direct mode operation for SW, MW and LW



3.1.3 DIVIDER FROM V_{CO} FREQUENCY TO REFERENCE FREQUENCY

This divider provides a low frequency f_{SYN} which is phase compared with the reference frequency f_{REF}. It is controlled by the registers PC0 to PC10 and SC0 to SC4

3.1.4 OPERATING MODE

Four operating modes are available:
- FM mode,
- AM swallow mode,
- AM direct mode,
- Standby mode

They are user programmable with the SWR/DIR and AM/FM registers.
Standby mode: (SWM/DIR = 0; AM/FM = 0):
Stopps all functions. This allows low current consumption without lost of information in all registers.

3.1.4.1 FM and AM (SW) Operation (Swallow Mode)

The FM or AM signal applies a two modulus: 32/33 prescaler, which is controlled by a 5 bit divider 'A'.The 5 bit SC register controls this divider. In parallel the output of the prescaler connectes a 11 bit divider 'B'. The 11 bit PC register controls this divider.

Dividing range calculation :
$f_{VCO} = [\ 33 \cdot A + (B + 1 - A) \cdot 32\ ] \cdot f_{REF}$
$f_{VCO} = (32 \cdot B + A + 32) \cdot f_{REF}$
Important: For correct operation $B \geq 32$ and $B \geq A$.
A and B are variable values of the dividers.

The AM signal applies directly to the 16 bit static divider 'C'. Both SC and PC registers contol this divider.
Dividing range: $f_{VCO} = (C + 1) \cdot f_{REF}$

3.1.4 REFERENCE FREQUENCY GENERATOR

The crystal oscillator clock is divided by the reference frequency divider to provide the reference frequency to the phase comparator. Reference frequency divider range is selectable by the programming bit 'f_{REF}'.
Available reference frequencies are shown in following table.

TABLE 3.4

AM/FM	$f_{REF\,2}$	$f_{REF\,1}$	f_{REF} (kHz)
0	1	1	6.25
0	1	0	12.50
0	0	1	25
0	0	0	50
1	1	1	1
1	1	0	2
1	0	1	2.50
1	0	0	5

3.1.5 THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator

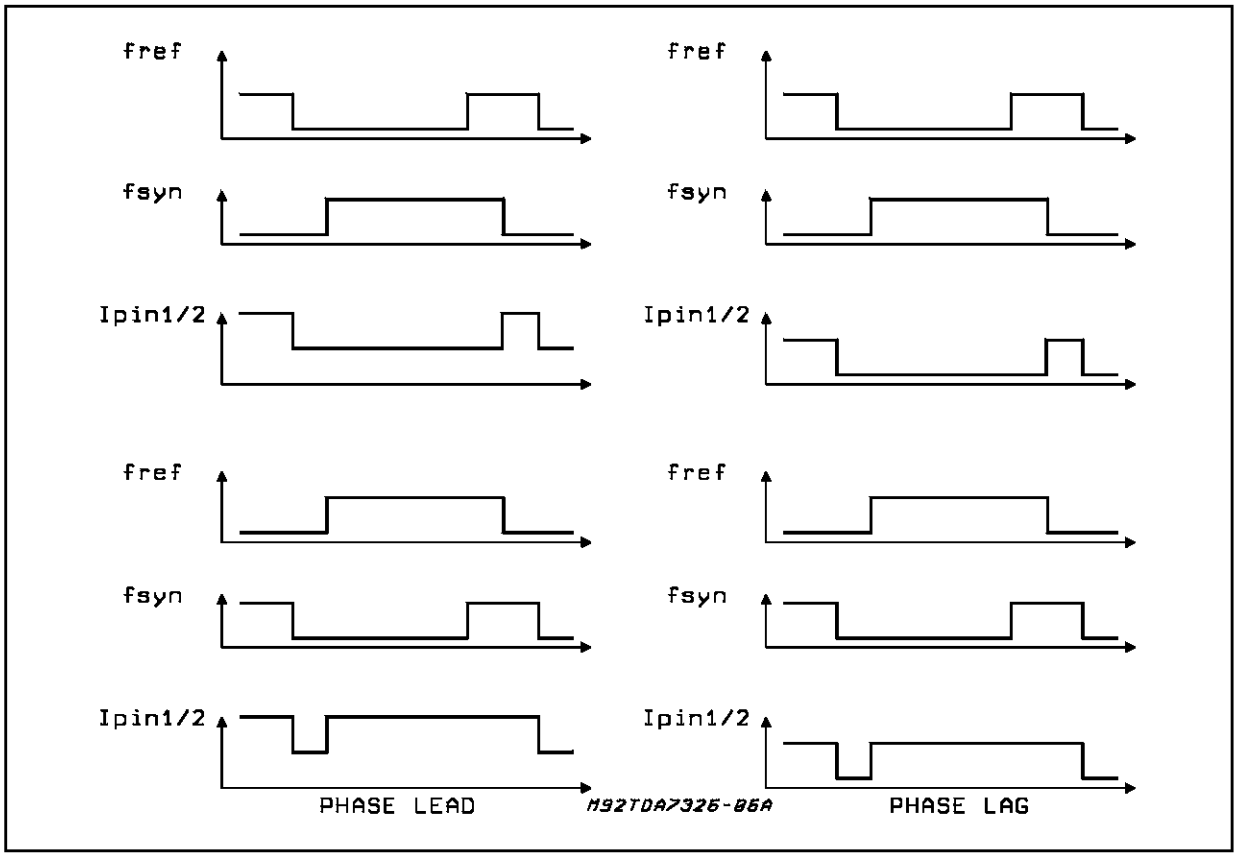
3.1.6 CHARGE PUMP CURRENT GENERATOR

This system generators signed pulses of current. Duration and polarity of those pulses are determined by the phase error signal. The absolute current values are programmable by 'CURR1' and 'CURR2' register and controlled by an external resistor R_{ISET} connected to Pin 3 and GND.

3.1.7 LOW NOISE CMOS OP-AMP

A low noise Op-Amp is available on chip. The

Figure 4: Phase comparator



positive input of this Op-Amp is connected to an internal voltage divider and to Pin 4 'V_{REF}'. The negative input is connected to the charge pump output.

In cooperation with this internal amplifier and external components, a active filter can be provided. To increase the flexibility in application the negative input can be switched to two input pins (Pins LPIN 1, LPIN 2). This switch is controlled by 'LPF' register with 'LPF' low LPIN 1is active and 'LPF' high LPIN 2 is active.

This feature allows two separate active filters with different performance.

3.2 THE IF COUNTER SYSTEM

3.2.1 Input Amplifier for the IF-Counter

Two separate amplifiers are generating a logical level. This signal drives the frequency dividers.

3.2.1.1 Input Impedance for the IF-Counter

Typical input impedance for IF-FM input is 2KΩ.

Typical input impedance for IF-AM input is 2KΩ.

3.2.2 Adjustment of the Measurement Sequence Time

The precision of the measurements is adjustable by controlling the discrimination window and the measurement time. During FM mode, the following values are available by programming the control registers "IFCA0" to "IFCA5" During AM and AM up-conversion mode, the discrimination window is fixed to 1KHz

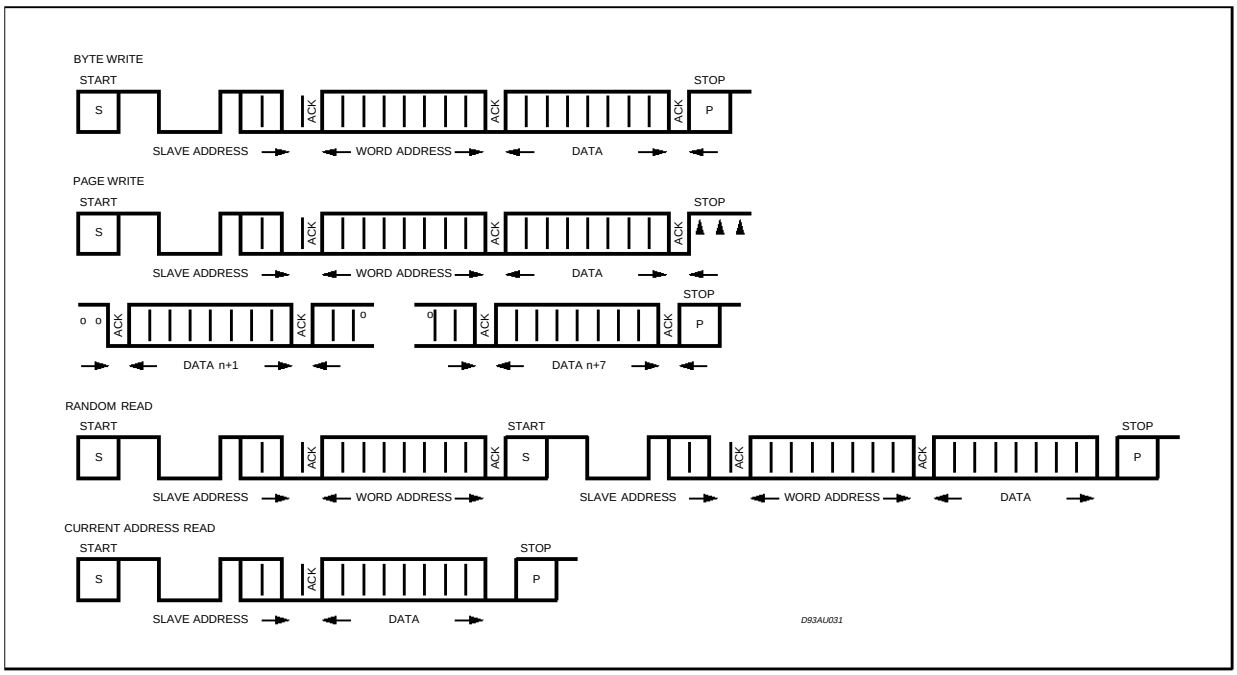
TABLE 3.2.2.2

IFCA			SAMPLING
5	**4**	**3**	**Time (msec)**
1	1	1	4
1	1	0	8
1	0	1	16
1	0	0	32
0	1	1	64
0	1	0	128

TABLE 3.2.2.1

IFCA			Discrimination Window (kHz)					
2	**1**	**0**	**sample time = 4ms**	**sample time = 8ms**	**sample time = 16ms**	**sample time = 32ms**	**sample time = 64ms**	**sample time = 128ms**
0	0	0		æ 400	± 200	± 100	± 50	± 25
0	0	1	± 400	± 200	± 100	± 50	± 25	± 2.5
0	1	0	± 200	± 100	± 50	± 25	± 12.5	± 6.25
0	1	1	± 100	± 50	± 25	± 12.5	± 6.25	
1	0	0	± 50	± 25	± 12.5	± 6.25		
1	0	1	± 25	± 12.5	± 6.25			
1	1	0	± 12.5	± 6.25				
1	1	1	± 6.25					

Figure 5: Bus Timing



3.2.3 Adjust of the Frequency Value

For the operation via the pin "IFIO", the center frequency of the discrimination window is adjustable by the control register "IFCB0" to "IFCB4". Available values are shown in tables 3.2.3.1, 3.2.3.2, 3.2.3.3.

For FM mode:

TABLE 3.2.3.1

PLL Control Register	IF Control Register					IF Centre Frequency
AM/FM	IFCB4	IFCB3	IFCB2	IFCB1	IFCB0	(MHz)
0	0	0	0	0	0	10.79375
0	0	0	0	0	1	10.78750
0	0	0	0	1	0	10.78125
0	0	0	0	1	1	10.77500
0	0	0	1	0	0	10.76875
0	0	0	1	0	1	10.76250
0	0	0	1	1	0	10.75650
0	0	0	1	1	1	10.75000
0	0	1	0	0	0	10.74375
0	0	1	0	0	1	10.73750
0	0	1	0	1	0	10.73125
0	0	1	0	1	1	10.72500
0	0	1	1	0	0	10.71875
0	0	1	1	0	1	10.71250
0	0	1	1	1	0	10.70625
0	0	1	1	1	1	10.70000
0	1	0	0	0	0	10.69375
0	1	0	0	0	1	10.68750
0	1	0	0	1	0	10.68125
0	1	0	0	1	1	10.67500
0	1	0	1	0	0	10.66875
0	1	0	1	0	1	10.66250
0	1	0	1	1	0	10.65625
0	1	0	1	1	1	10.65000
0	1	0	0	0	0	10.64375
0	1	0	0	0	1	10.63750
0	1	0	0	1	0	10.63125
0	1	0	0	1	1	10.62500
0	1	0	1	0	0	10.61875
0	1	0	1	0	1	10.61250
0	1	0	1	1	0	10.60625
0	1	0	1	1	1	10.60000

TABLE 3.2.3.2: For AM Up-conversion Mode

PLL Control Register	IF Control Register					IF Centre Frequency
AM/FM	IFCB4	IFCB3	IFCB2	IFCB1	IFCB0	(MHz)
1	0	0	0	0	0	10.708
1	0	0	0	0	1	10.707
1	0	0	0	1	0	10.706
1	0	0	0	1	1	10.705
1	0	0	1	0	0	10.704
1	0	0	1	0	1	10.703
1	0	0	1	1	0	10.702
1	0	0	1	1	1	10.701
1	0	1	0	0	0	10.700
1	0	1	0	0	1	10.699
1	0	1	0	1	0	10.698
1	0	1	0	1	1	10.697
1	0	1	1	0	0	10.696
1	0	1	1	0	1	10.695
1	0	1	1	1	0	10.694
1	0	1	1	1	1	10.693

TABLE 3.2.3.3: For AM Normal Mode

PLL Control Register	IF Control Register					IF Centre Frequency
AM/FM	IFCB4	IFCB3	IFCB2	IFCB1	IFCB0	(KHz)
1	0	0	0	0	0	468
1	0	0	0	0	1	467
1	0	0	0	1	0	466
1	0	0	0	1	1	465
1	0	0	1	0	0	464
1	0	0	1	0	1	463
1	0	0	1	1	0	462
1	0	0	1	1	1	461
1	0	1	0	0	0	460
1	0	1	0	0	1	459
1	0	1	0	1	0	458
1	0	1	0	1	1	457
1	0	1	1	0	0	456
1	0	1	1	0	1	455
1	0	1	1	1	0	454
1	0	1	1	1	1	453
1	1	0	0	0	0	452
1	1	0	0	0	1	451
1	1	0	0	1	0	450

3.2.4 Starting the Counter

A high low transition at pin "IFIO" or setting the bit IFS7 of the status register "IFS" to LOW will start the count of the supplied IF frequency at pin "IF-FM" or " IF-AM". It depends on the status of the control register ÄM/FM" Pin "IFIO" is switched to forcing low level. After a successful evaluation, the device will switch the "IFIO", pin in tristate condition.
If no valid result is detected, a new measurement automatically will be started. This will be done until a valid counter result is detected. The measurement can be stopped by setting bit 7 of the status register " IFS" to HIHG.

3.2.4.1 Transfer of the Absolute Counter Values After the Conversion

The absolute state of the internal counter is available as a serial information located in the register "IFS".
The bit organization of the 8 bit register "IFS" is shown in table 3.2.4.

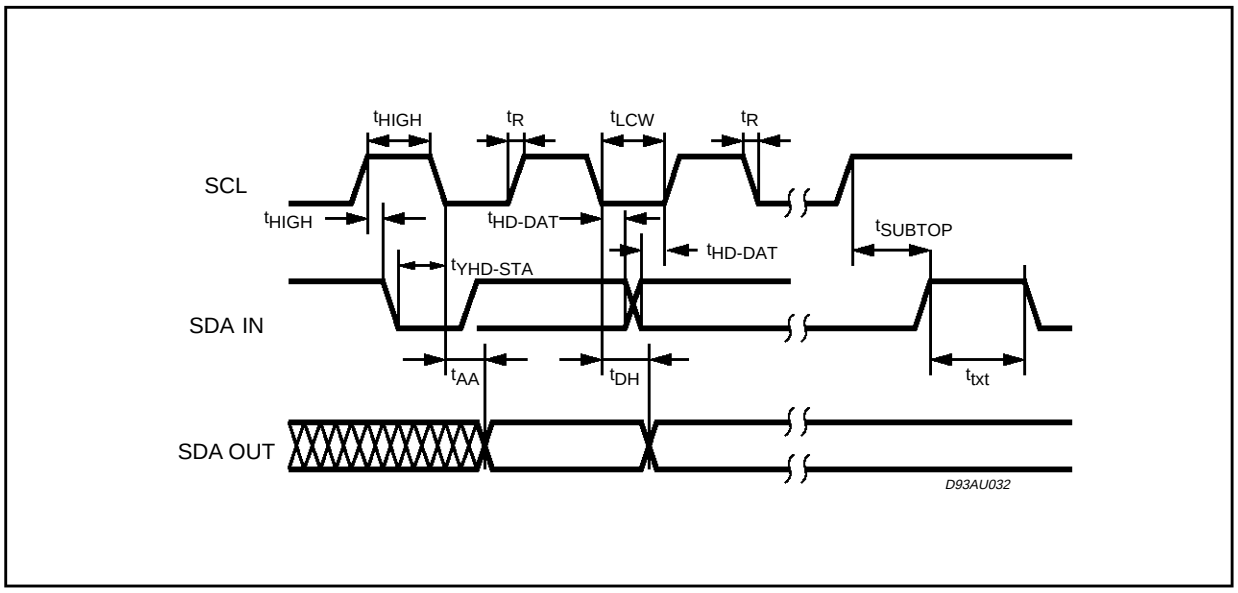
TABLE 3.2.4

IFS 7	STATUS: 1 = BUSY; 0 = READY
IFS 6	OVERFLOW: 1 = OVERFLOW
IFS 5	PREFIX: 1 = NEGATIVE
IFS 4	IF COUNTER 4
IFS 3	IF COUNTER 3
IFS 2	IF COUNTER 2
IFS 1	IF COUNTER 1
IFS 0	IF COUNTER 0

EXAMPLES:

Counter Status	IFS Register							
IF Counter	IFS 7	IFS 6	IFS 5	IFS 4	IFS 3	IFS 2	IFS 1	IFS 0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
-1	0	0	1	1	1	1	1	1
-2	0	0	1	1	1	1	1	0
31	0	0	0	1	1	1	1	1
-32	0	0	1	0	0	0	0	0
70	0	1	0	0	0	1	1	0

Figure 6: Timing Diagram



3.3 GENERAL PARTS OF THE DEVICE

3.3.1 Switch Outputs

At the 20 pin version, two digital outputs DOUT1 and DOUT0 digital n-channel open drain outputs are available in application mode. At the 28 pin version 9 digital n-channel open drain outputs "DOUT0" to "DOUT8" are available. This outputs are controlled by the "DOUT"-registers.

3.4 PC-BUS INTERFACE

The TDA7327 supports the I^2C bus protocol. This protocol defines any device that sends data into the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations.

Data Transition:

Data transition on the SDA line must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as START or STOP condition.

Start Condition:

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The TDA7327 continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

Stop Condition:

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus interface of the TDA7327 into the initial condition.

Acknowledge:

Suggest a successful data transfer. The transmitter will release the bus after sending 8 bit of data, during the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it has received the eight bits of data, correctly.

Data transfer:

During data transfer the TDA7327 samples the SDA line on the leading edge of the SCL clock. Thre fore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

3.4.1 Device Addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing.
The most significant 6 bits of the slave address are the device type identifier.

The TDA7327 frequency synthesizer device type is fixed as "110001".

The next significant bit is used to address a particular device of the previous defined type connected to the bus. The state of the hardwired A0 pin defines the state of this address bit. So up to two devices could be connected on the same bus.
The last bit of the instruction defines the type of operation to be performed:
- When set to "1", a read operation is selected
- When set to "0", a write operation is selected

The communication begins with a START condition followed by chip address byte.
All devices connected to the bus will compare their own hardwired address with the slave address being transmitted.
After this comparison, the TDA7327 will acknowledge on the SDA line and will perform either a read or write operation according to the state of R/W bit.

3.4.2 Write Operation

Following a START condition the master sends a slave addressword with the R/W bit set to "0". The TDA7327 will acknowledge this first transmission and waits for a second word (the word address field).
This 8 bit address field provides an access to any of the 8 internal addresses. Upon receipt of the word address the TDA7327 slave device will respond with an acknowledge. at this time, all the following words transmitted to the TDA7327 will be considered as Data. the internal addresswill be automatically incremented. After each word receipt the TDA7327 will answer with an acknowledge.

3.4.3 Read Operation

The read mode operaton allows the master to access the status bite of the IF counter system. In order to load into the device the address, the master must first perform a "dummy" write sequence. (START, slave address with R/W bit set to "0", followed by the word address).
After the word address has been acknowledged, the master immediately reissues a START instruction with the R/W bit set to "1". The TDA7327 will acknowledge the transfer and output the 8 bit data. To terminate this transfer the master must not acknowledge the transfer and does generate a STOP instruction.

ADDRESS

1	0	1	0	0	1	A	R/W

0 = WIRE
1 = READ
A = STATUS ADDRESS PIN (pin 5)

Figure 7: Application with two loopfilters and V_{tun} <10V

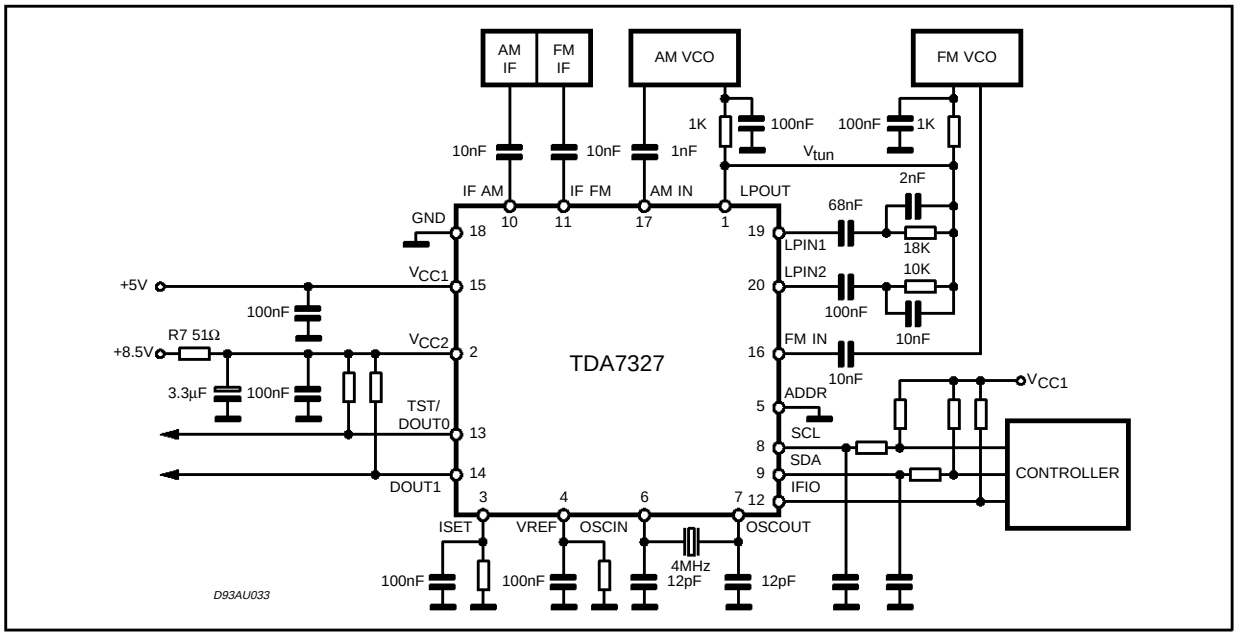
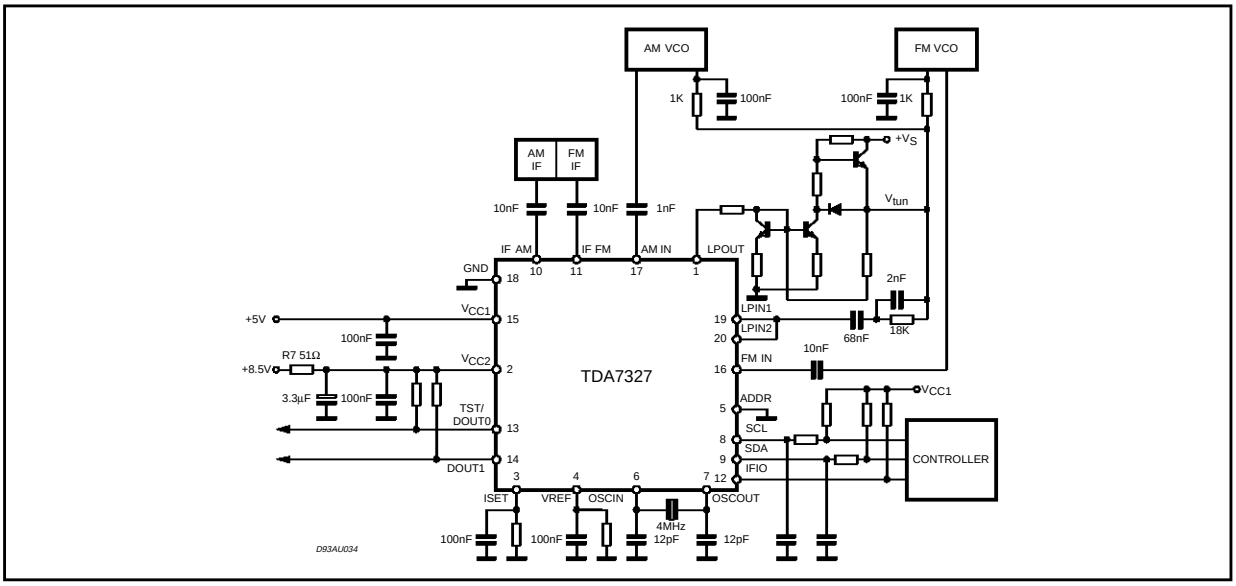
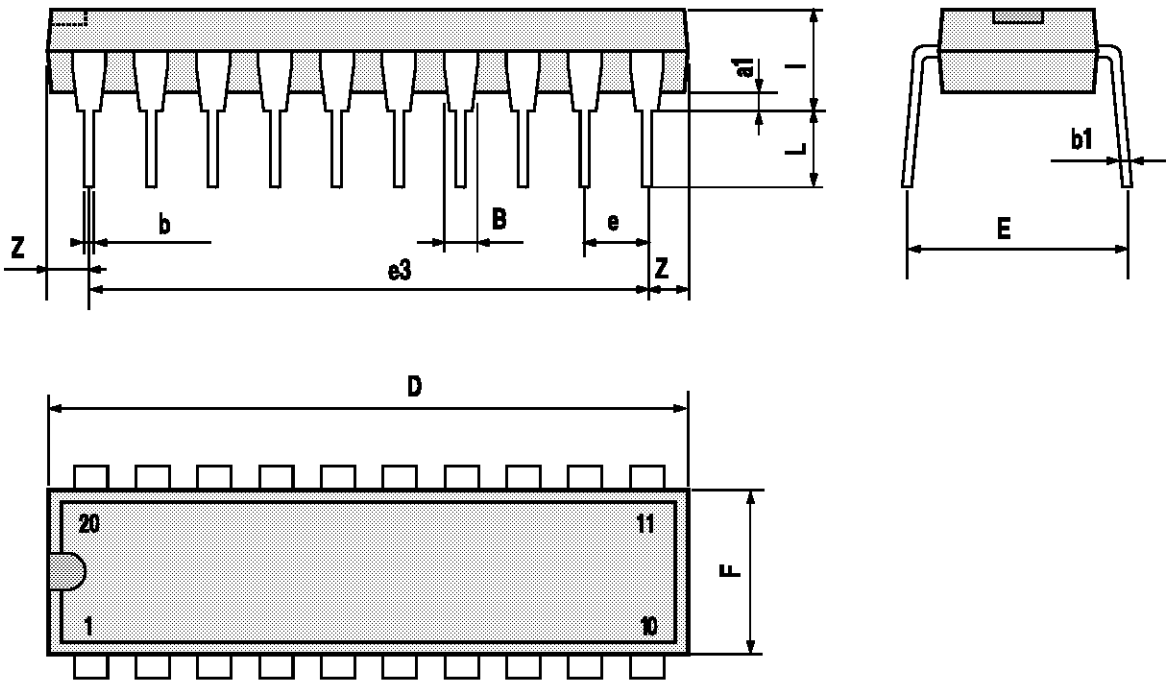


Figure 8: Application with single loopfilters and V_{tun} >10V



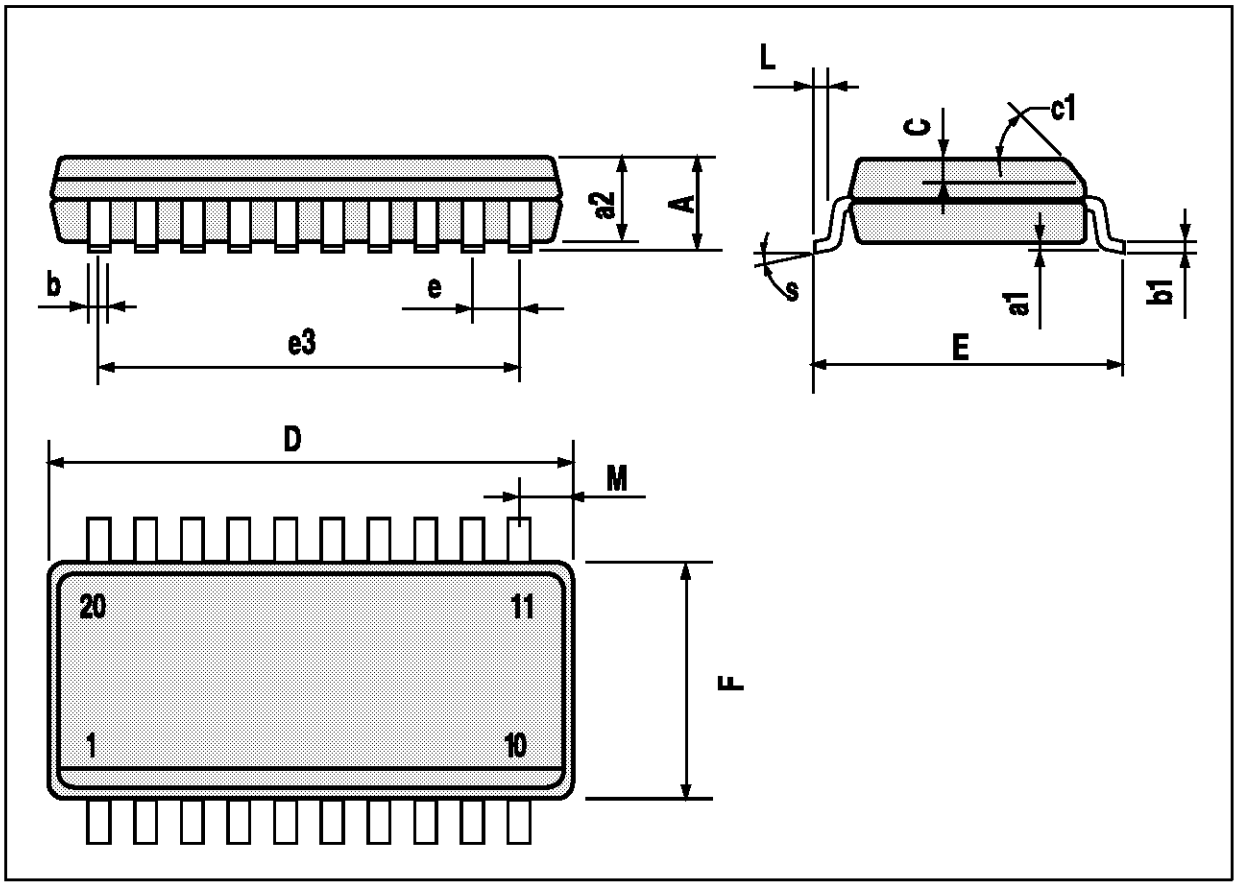
DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					



SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)